**[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)**

**15210**

**B. Tech 6th Semester Examination**

**Computer Architecture (OS)**

**EC-6001**

**Time : 3 Hours** **Max. Marks : 100**

*The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.*

**Note :** Attempt five questions in all selecting one from each of sections A, B, C and D. Section E is compulsory.

## SECTION - A

1. (a) Define addressing modes. Classify addressing modes and explain each type with example. (10)

   (b) Describe in detail Booths algorithm for binary multiplication and its hardware implementation. (10)

2. (a) Explain the architecture of basic computer with neat and clean diagram and proper labeling. (10)

   (b) Differentiate hardwired control unit with microprogrammed unit depicting merits and demerits. (10)

## SECTION - B

3. (a) Explain the concept of locality principle, hit ratio and effective access time w.r.t cache. (10)

   (b) Explain all kinds of memories used in computer system with their technical specifications. (10)





4. (a) What do you understand by CAM and memory interleaving and why these are being used in computer systems? (10)

   (b) A Virtual memory has a page size of 1 K words. There are eight pages and four blocks. The associative memory page table contains the following entries:

| Page | Block |
|---|---|
| 0 | 3 |
| 1 | 1 |
| 4 | 2 |
| 6 | 0 |

   Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU. (10)

## SECTION - C

5. (a) What are various inter communication methodologies used in computer system to access I/O devices? Explain with suitable examples. (10)

   (b) Explain various Serial and parallel bus architectures with example and their usage. (10)

6. (a) What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? (10)

   (b) Explain any four computer peripherals used in computer system as an output device with their specifications and merits over others. (10)

## SECTION - D

7. (a) Determine the number of clock cycles that it takes to process 100 tasks in a four segment pipeline and also calculate the speed up factor. (10)

   (b) Explain any three major difficulties that cause the instruction pipeline to deviate from its normal operation. (10)

8. (a) Draw the space time diagram for a six segment pipeline showing the time it takes to process eight tasks. Derive the expression for speed up in pipelining. (10)

   (b) What are the various hurdles we face in implementing the pipeline processors? (10)

## SECTION - E

9. (a) Explain Flyns Taxonomy in brief.

   (b) How many memory chips of (256x8) are needed to provide a memory capacity of 4096x16?

   (c) What is a system bus model?

   (d) Differentiate USB with Firewire technologies.

   (e) Explain all transmission modes.

   (f) What is ROM and how it is further classified?

   (g) What is cache coherence and how it is eliminated?

   (h) Explain vectored interrupts.

   (i) Explain any two branch instructions.

   (j) What are super pipelined and super scalar machines? (2×10=20)